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PATENT ABSTRACTS OF JAPAN

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(71) Applicant: **NEC CORP**

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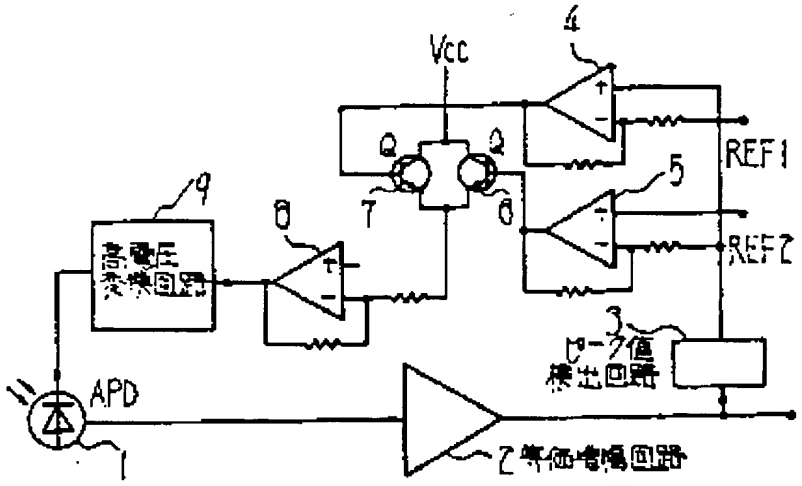
(74) Representative:

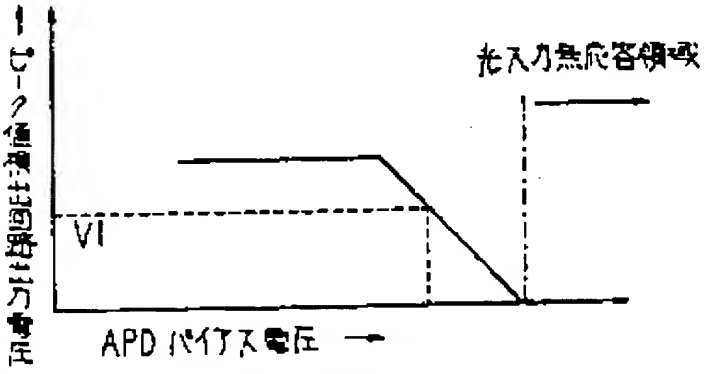
(54) APD BIAS VOLTAGE CONTROL METHOD

(57) Abstract:

PURPOSE: To eliminate a maximum voltage control circuit and to decrease the time constant of an APD bias voltage control circuit by a method wherein loop control is established so that excessive bias voltage is not applied to an avalanche photodiode (APD) even if an optical input signal is off.

CONSTITUTION: The reference voltage(REF1) of an operational amplifier 4 is adjusted so that the output amplitude of an equivalent amplifying circuit 2 at the time of optical signal input may be the specified value. Moreover, the reference voltage(REF2) of the operational amplifier is adjusted so that the output voltage of a peak value detecting circuit 3 may be the voltage V1. If there is optical input, the output amplitude of the equivalent amplifying circuit 2 becomes constant by the feedback loop composed of the peak value detecting circuit 3, an operation amplifier 4, a transistor Q7, an operational amplifier 8, and a high voltage converting circuit 9.





Moreover, when optical input becomes off, APD bias voltage becomes the voltage determined by the V1 since the negative feedback loop is established, from the relation between the APD bias voltage at the time of optical input being off and the peak value detecting circuit output voltage, of the loop composed of the peak value detecting circuit 3, an operation amplifier 5, a transistor Q6, an operation amplifier 8, and a high voltage converting circuit 9.